APPLICATIONS OF JOSEPHSON PROCESSOR TECHNOLOGY*

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ABSTRACT

Several future Navy signal processing applications were analyzed, and the computation requirements quantified. The anticipated performance of Josephson logic and memory devices was incorporated into a processor sizing model, and Josephson processor configurations estimated.

INTRODUCTION

A study was undertaken to evaluate the potential applicability of Josephson processor technology to Navy future signal processing needs. Packaging concepts and circuit speeds for Josephson logic and memory were extrapolated to a set of Josephson processor characteristics. Several applications were subsequently analyzed and the computational requirements determined. These requirements then formed the basis for estimating Josephson Processor sizes for the various applications considered.

SUMMARY

The research and development program in Josephson technology underway at the IBM Research Division facilities in Yorktown Heights and Zurich is exploring the complete span of technology from materials and device characteristics through packaging and testing concepts. Information on the technology, including materials, circuits and performance, has been presented in recent references 1 - 14, and is also the subject of several papers in the Gigabit Logic Conference held in conjunction with this Symposium. The major milestone of the IBM project is a Prototype Josephson Signal Processor (PJSP). The purpose of the PJSP is to demonstrate the feasibility of Josephson technology for high performance computer applications. Based on dimensions and delays of experimental logic and memory circuits and a novel package concept, the following target values have been used for this study: a processor with approximately 4000 logic circuits and approximately 32K bytes of memory fitting into less than 25 cm^3, dissipating approximately 150 mW and exhibiting a cycle time of approximately 2.5 ns. These target values were extended to larger processors for this study.

The study emphasized computationally intensive signal processing applications with an attempt to include (1) a range of platforms from submarines to satellites, (2) both open and closed cycle cryocooler missions, and (3) a range of problems requiring a range of processor performance. Using this criteria, five applications were analyzed. Computational requirements were estimated in million multiples per second (mmps) and Josephson processors sized for each application, both in terms of numbers of PJSPs needed (assuming the existence of an unspecified paralleling scheme and algorithms improvements) and in terms of a Josephson processor designed for each application.

The five applications analyzed included two in the radar area, Synthetic Aperature Radar(SAR) and Airborne Early Warning (AEW) radar, two in the acoustic area, Advanced Submarine Sonar and Underseas Surveillance, and one in the Electronic Support Measure (ESM) area. Scenarios were postulated for each of these applications for purposes of illustrating the situation and to develop the signal processing needs. The SAR application involves a satellite-borne radar to locate and identify ships for an Over-the-Horizon targeting system. The AEW radar involves an aircraft radar for detection and tracking of aircraft, missiles and ships. The Advanced Submarine Sonar is a projected future generation attack submarine acoustic system, and the Underseas Surveillance system assumes interarray correlation for ocean basin coverage. The ESM application involves emitter detection and intrapulse modulation pulse processing.

Computation and memory requirements were estimated for each of these applications (Table 1, Columns 1 through 4) and related to the anticipated performance of the PJSP (Table 1, Column 5). A generalized Josephson processor sizing algorithm was developed and the results of applying it to the requirements are shown in the last columns of Table 1. As noted, the requirements range from 140 to 7290 million multiples per second and the resulting Josephson processors range in size from 138 to 1100 cm^3 and power consumption from under 0.5 watts to 5.36. Input/output circuits and cryocooler needs are not included. For perspective, cryocoolers were estimated, and an airborne unit for the ESM application might weigh 55 kg, require a volume of 70,000 cm^3 and have a power input of 2900 watts.

The enormous capability of Josephson technology processors has been illustrated by the results of this study, which was sponsored in part by the Office of Naval Research.

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Table 1. Josephson Processor Technology Applications

Application	Processing Requirements				PJSPs Required	Josephson Processor	
	Throughput (mmps)	Main Memory (K Bytes)	Cache Memory (K Bytes)	ROM Memory (K Bytes)		Volume (cm^3)	Power (W)
SAR Radar	140	2,000	64	64	4	138	0.42
AEW Radar	7290	12,000	64	128	161	828	5.36
Advanced Submarine Sonar	570	20,000	64	128	14	1100	1.1
Interarray Processing	1600	2,000	128	64	42	192	1.64
ESM	2500	256	256	128	65	170	2.7

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